

**ChipGlobe GmbH**  
**Volker Frisch, CEO**



[www.chipglobe.com](http://www.chipglobe.com)

# Our Identity - Vision, Mission, Values, Company



## ChipGlobe in a nutshell

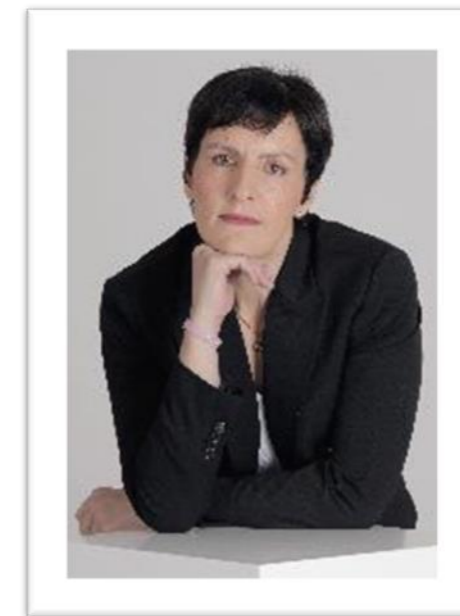
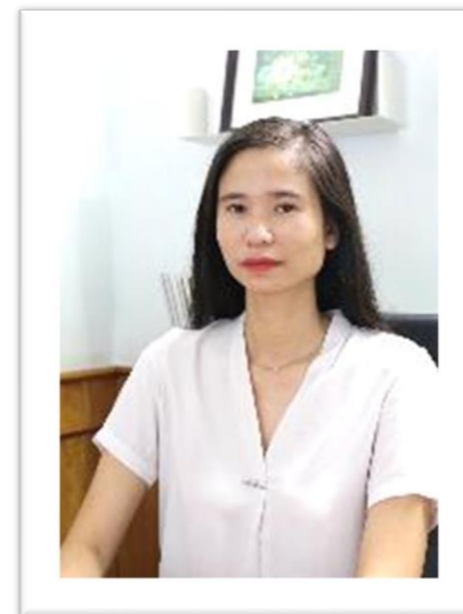
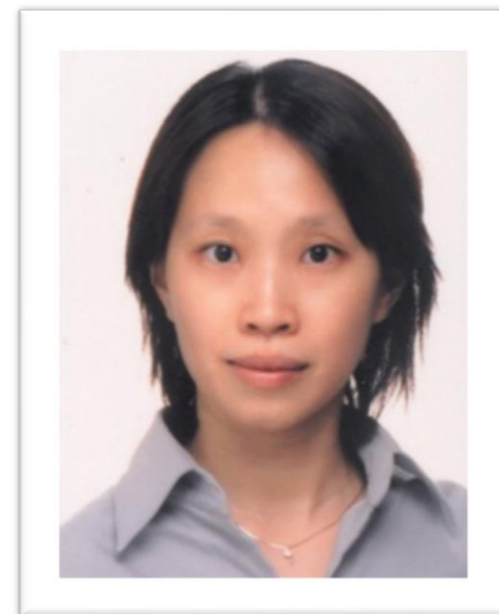
- ASIC /RTL2GDS & Functional Verification, RTL Design, Test Engineering, Firmware, FPGA, and Embedded System development from idea to prototype
- 15+ years of successful long-term project expertise and excellent QoR with Global Semiconductor Companies. Long term and good relationships in projects
- More than 100 senior experts
- Working successfully with our customers with ChipGlobe ODC Model
- Embedded Systems Solution Provider: Infineon Security Partner Network (ISPN) + Infineon Design House



## Company Profile – Management Team



### Diverse Management Team at ChipGlobe



**Roland Klemt**

Managing Director

ChipGlobe Germany GmbH

**Volker Frisch**

CEO

**Lay Suan Ng**

Managing Director

ChipGlobe Asia Pacific Pte. Ltd.

**Elizabeth Ngo**

Managing Director

ChipGlobe Vietnam Co., Ltd.

**Marija Ugarak**

Managing Director

ChipGlobe d.o.o Beograd

&

ChipGlobe Greece MIKE

#### ChipGlobe GmbH

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#### Office Address (ODC):

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85579 Neubiberg, Munich  
Germany

#### ChipGlobe Asia Pacific Pte. Ltd. (ODC)

25 International Business Park #04-64  
German Centre  
Singapore 609916

#### ChipGlobe d.o.o Beograd (ODC)

Milutina Milankovića 11v  
11070 Belgrade. Serbia  
GREEN HEART – Building N3, 5th floor

#### ChipGlobe Greece MIKE (ODC)

Karatasou 7  
54626 Thessaloniki, Greece

#### ChipGlobe Vietnam Co., Ltd.

36/10 Nguyen Gia Tri  
Ward 25, Binh Thanh District  
Ho Chi Minh City  
Vietnam

# ChipGlobe Locations & Focus Areas

## ChipGlobe Design Center Focus Areas

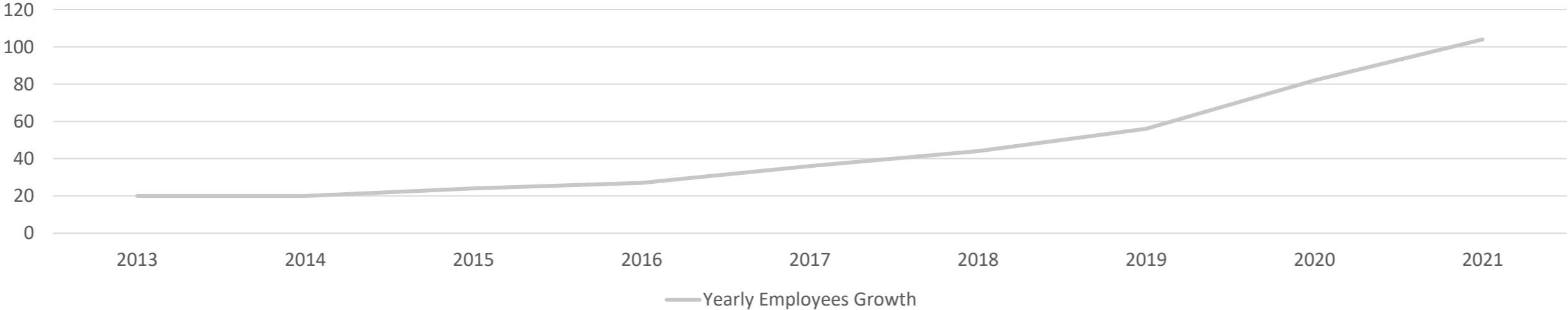
ODC - Neubiberg/Munich/Dresden – Germany	
Now	RTL2GDS, Funct. Verification, RTL Design, Firmware, Analog Layout, DFT, Test Engineering Program Management, FMEA
Roadmap	RF, ISO26262 expert, PgMP®, PMP®
ODC – Singapore	
Now	RTL2GDS, Functional Verification, RTL Design, Program Management
ODC – Belgrade – Serbia	
Now	Functional Verification, RTL Design, Firmware, TLM, Program Management, Application Boards, Mixed Signal Verification
Roadmap	RF, DFT, RTL2GDS, Tester Engineering
ODC – Ho Chi Minh, Vietnam	
Now	RTL2GDS, Functional Verification, RTL Design, DFT, Firmware, Test Engineering
ODC – Thessaloniki - Greece	
Now	Functional Verification, RTL Design, Mixed Signal Verification
Roadmap	DFT, RTL2GDS, Tester Engineering



# ChipGlobe History



Yearly Employees Growth





- ChipGlobe ODC Belgrade opened in April 2017 with office space for 30 engineers.
- Moved to new office space in May 2020 – space for 60 engineers.
- Successful Ramp up of the ODC aligned with Infineon and customer expectations.
- **Focus: Functional Verification, RTL Design, Firmware Verification and Firmware/Embedded Systems Design**
- Successful project involvement with Infineon in Munich and other global semiconductor companies in multiple projects
- **Focus on senior and expert engineers.**
- Internship program established + cooperation with technical university Belgrade finalized to support the hiring of junior engineers
  - Focus on Functional Verification and RTL Design in internships





Management Service

## CERTIFICATE

The Certification Body  
of TÜV SÜD Management Service GmbH  
certifies that



**Chipglobe GmbH**  
- site representative -

Cincinnati-Str. 60, 81549 München  
Germany

at the site

Professor-Messerschmitt-Str. 1, 85579 Neubiberg  
Germany

has established and applies  
a Quality Management System for

**Provision of  
engineering services for customers in the area  
of System-on-Chip-Solutions.**

An audit was performed, Order No. 707102988.

Proof has been furnished that the requirements  
according to

**ISO 9001:2015**

are fulfilled.

The certificate is valid from 2020-01-03 until 2023-01-02.

Certificate Registration No.: 12 100 59293 TMS.

*E. Koller*

Product Compliance Management  
Munich, 2020-01-03



**ISO 9001**

Certified  
Quality Management System

[www.tuv-sud.com/ms-cert](http://www.tuv-sud.com/ms-cert)

[www.tuev-sued.de/ms-zert](http://www.tuev-sued.de/ms-zert)

ZERTIFIKAT ◆ CERTIFICATE ◆ 認 證 證 書 ◆ CERTIFICADO ◆ CERTIFICAT





# ChipGlobe Focus Areas Technically

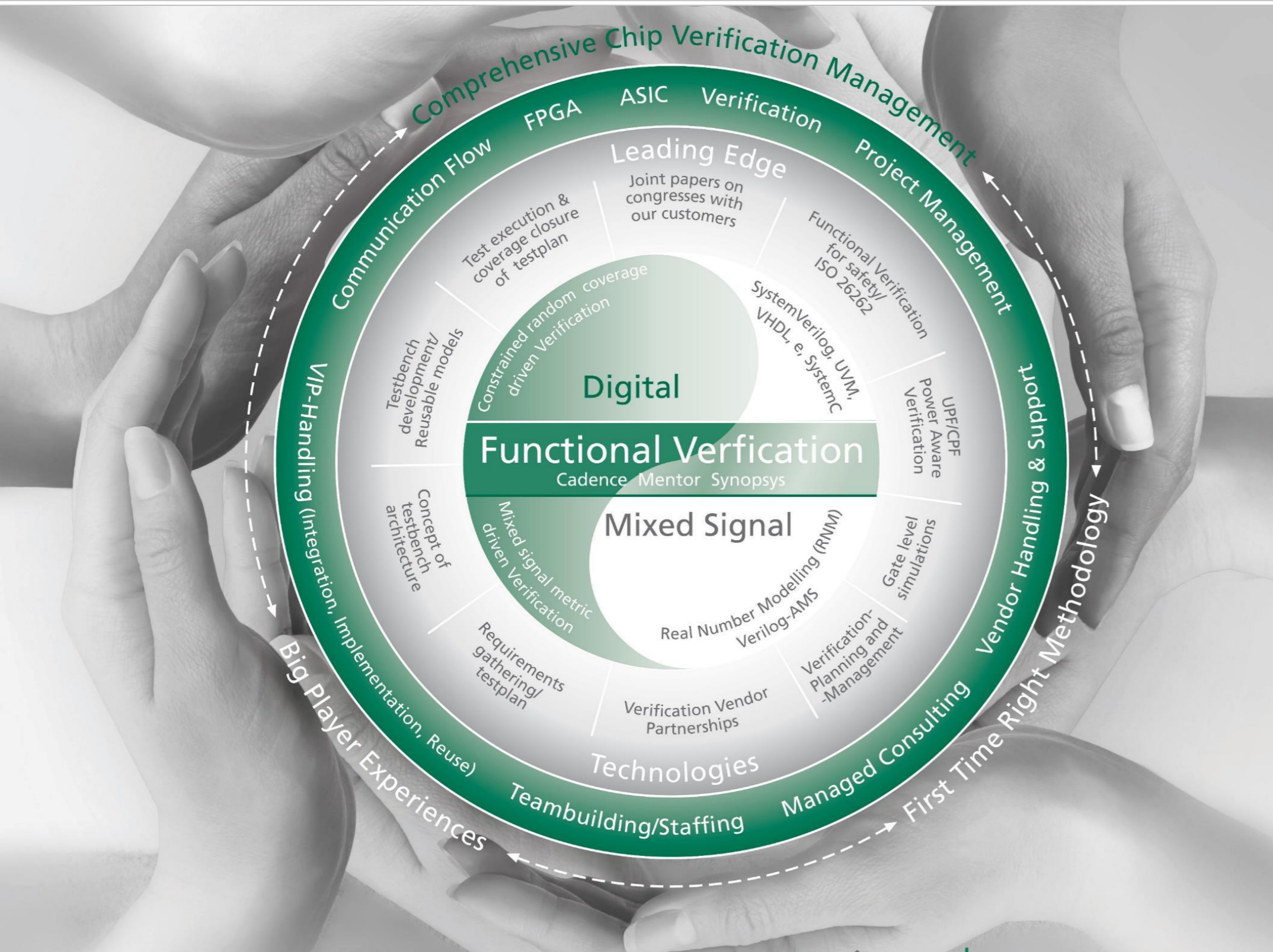


- Working from ODCs in Munich, Belgrade, and Ho Chi Minh City – managed by ChipGlobe Onsite Manager
- Onsite sync meetings / ramp-up at customer sites
- Well-working teams enable large and complex tasks and designs
- Complementing major semiconductor companies' R&D teams





# Functional Verification



- Broad and deep expertise in SystemVerilog and UVM
- From setup of testbench architecture to Module and Top Level Verification
- Proven Setup with Onsite Manager/Teamlead @ customer site and setup with Offshore ODC teams and VPN integration.

# Skillset Functional Verification Team



Functional and Mixed Signal Verification	
<b>Verification Languages</b>	<ul style="list-style-type: none"><li>• Specman e, eVC development</li><li>• System C, C++, TLM (Transaction Level Modelling)</li><li>• SystemVerilog / RNM (Real Number Modelling)</li><li>• Verilog</li><li>• Verilog-AMS</li><li>• VHDL</li></ul>
<b>Verification Methodologies</b>	<ul style="list-style-type: none"><li>• Constraint random coverage driven verification</li><li>• Mixed signal metric driven verification</li><li>• SoC + IP level verification</li><li>• Gate level verification</li><li>• Firmware verification</li><li>• Portable stimulus (in rampup together with Mentor)</li><li>• Secure designs and verification based on ISO 26262</li><li>• UVM / OVM</li></ul>
<b>Power Aware Verification</b>	<ul style="list-style-type: none"><li>• CPF</li><li>• IEEE 1801 / UPF</li><li>• UPF low power verification</li></ul>
<b>Verification Partnerships</b>	<ul style="list-style-type: none"><li>• Mentor Questa® Vanguard Partnership and Open Door Partnership Member</li><li>• Tool Independent Expertise in Projects with Cadence, Mentor + Synopsys Environments</li></ul>
<b>EDA Vendor Tool</b>	<ul style="list-style-type: none"><li>• Cadence, Mentor, Synopsys, JIRA and other bug/issue tracking tools</li></ul>





## Different Levels and Approaches

Our verification experts are always ready for the next challenge, whether it is a verification process starting from the device concept phase, defining and executing a methodology transition, or performing upgrades, maintenance, and support. Starting from the module level and all the way through to the SoC level of verification, we are offering structured and documented project execution providing limitless possibilities for re-use and upgrades in the next product cycles.

- Verification environment development/transition/upgrade
- Test development, transition, and/or upgrade
- 3<sup>rd</sup> party VIP usage and/or VIP development
- Metric-driven functional verification
- Coverage closure



# Skillset Design Service Team



Design Service / RTL Design	
<b>Languages</b>	<ul style="list-style-type: none"><li>• VHDL</li><li>• Verilog</li><li>• SystemVerilog</li><li>• Perl, TCL, Makefile and Python scripting</li></ul>
<b>Design categories</b>	<ul style="list-style-type: none"><li>• RTL design</li><li>• Lint, CDC and RDC checks</li><li>• Synthesis</li><li>• Logic equivalence checks (LEC)</li><li>• Functional safety (ISO 26262)</li></ul>
<b>EDA Vendor Tool</b>	<ul style="list-style-type: none"><li>• Cadence</li><li>• Synopsys</li><li>• Mentor</li><li>• JIRA and other bug/issue tracking tools</li></ul>



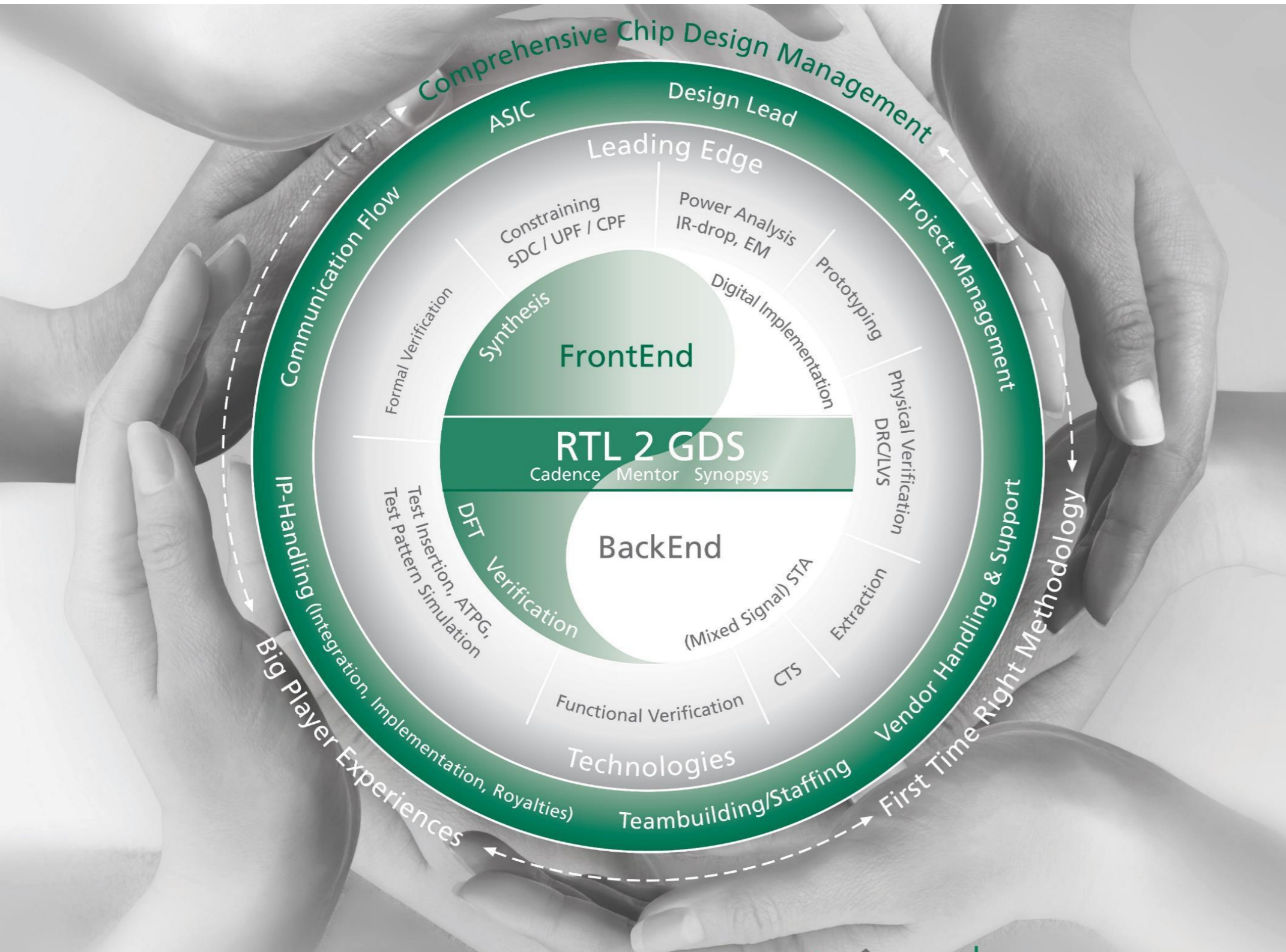


## Different Levels and Approaches

- Our design experts are always ready to share their experience and help to start from the device concept phase through defining safety mechanisms to the final sign-off timing closure phase.
- The optimal IP architectures and microarchitectures which save time during development and maintenance cycles are products of our experienced design engineers.
- Our designers always take care of the trade-off against area, power, effort, and performance.
- Having experience in working on projects with various clients our design team offers support for design flow and methodology improvements.
- Last, but not least important, our designers provide structured and documented RTL designs with limitless possibilities for reuse and upgrades in the next product generations.
- Our digital design engineers have exceptional problem-solving and analytical skills and always look at the big picture. Moreover, they deal with their daily work in a pragmatic and enthusiastic way and communicate clearly and openly.



# RTL2GDS – Synthesis and Layout



- Experience with 5nm, 7nm, 14nm, 16nm, and 28 nm technology nodes
- Deep experience with Cadence + Synopsys Flows /Tools + Mentor for DFT



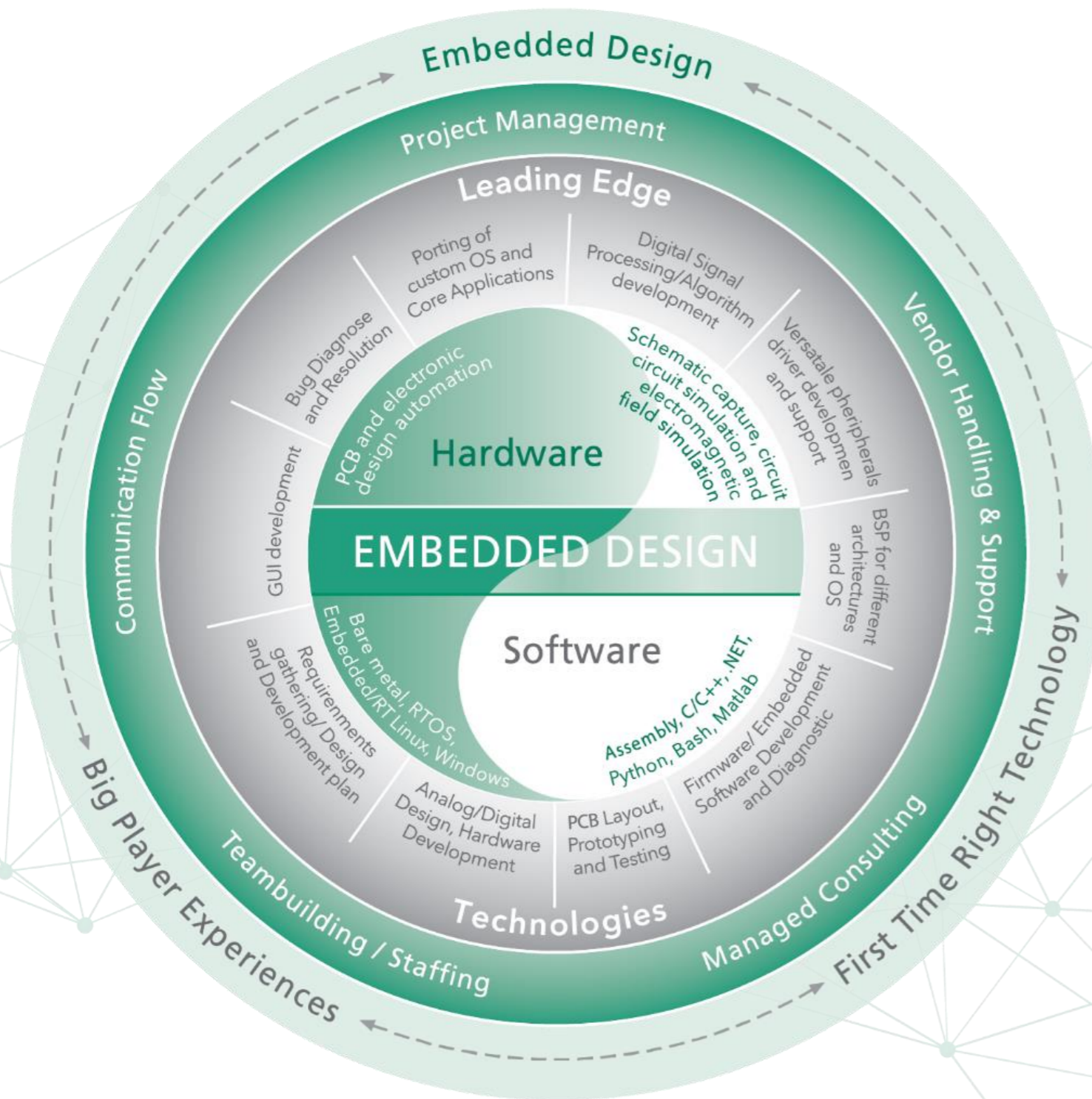
# ChipGlobe expert knowledge matrix

ChipGlobe Implementation – Design and Physical Verification (Tool independent expertise in projects for ANSYS, Cadence, Mentor Graphics and Synopsys environments)	
<b>Specification</b>	Vision
<b>RTL Coding</b>	VHDL, Verilog, SystemVerilog
<b>Linting, CDC Analysis</b>	<b>Cadence</b> ® JasperGold® , Incisive® Enterprise Simulator (HAL), Conformal® Constraint Designer <b>Synopsys</b> ® SpyGlass®, SpyGlass® CDC
<b>Synthesis</b>	<b>Cadence</b> ® Genus™ Synthesis (RTL Compiler), First Encounter® <b>Synopsys</b> ® Design Compiler®
<b>STA</b> (Top Level, hierarchical design, macro level)	<b>Cadence</b> ® Tempus™ <b>Synopsys</b> ® PrimeTime®, MSSTA (mixed signal)
<b>Dft, ATPG</b>	<b>Cadence</b> ® Genus™ (RTL Compiler), Modus™ test, Conformal®, Incisive® Enterprise Simulator <b>Mentor Graphics</b> ® DFT Advisor, BSD Architect, MBISTArchitect™, LBISTArchitect™, <b>Graphics</b> ® Tessent® Testkompres® , Fastscan™, Modelsim® <b>Synopsys</b> ® DFT Compiler/DFTMAX™, TetraMAX®, VCS®, TetraMAX® LBIST
<b>Formal Verification</b>	<b>Cadence</b> ® Conformal® Equivalence Checker, Conformal® Low Power <b>Synopsys</b> ® Formality®
<b>Floorplanning</b>	<b>Cadence</b> ® First Encounter® <b>Synopsys</b> ® IC Compiler™(ICC)
<b>Physical Implementation</b>	<b>Cadence</b> ® Innovus™ (Encounter®) <b>Synopsys</b> ® IC Compiler™ (ICC, ICC2)
<b>Extraction</b>	<b>Cadence</b> ® Quantus™ QRC <b>Synopsys</b> ® Star-RCXT™
<b>Physical Verification (DRC, LVS)</b>	<b>Cadence</b> ® Physical Verification System (PVS) <b>Mentor Graphics</b> ® Calibre® <b>Synopsys</b> ® ICV / Hercules™
<b>Power Analysis - Power Consumption, IR Drop Analysis, EM Analysis</b>	<b>ANSYS</b> ® ANSYS® Redhawk™ <b>Cadence</b> ® Voltus™ <b>Synopsys</b> ® Primerail

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# ChipGlobe Focus Embedded Design



- Working from ODCs in Munich and Belgrade – managed by ChipGlobe Onsite Manager
- Onsite sync meetings/ramp-up at customer sites
- Well-working teams enable large and complex tasks and designs
- ISPN Preferred Partner (Infineon Security Partner Network)
- Creation of customized demonstrator boxes with customer-specific hardware, software, and cloud integration (IoT, Security, Hardware Encryption, Sensors, AWS)

# Skillset Firmware Team



Design Service / RTL Design	
<b>Languages</b>	<ul style="list-style-type: none"><li>• Assembly languages</li><li>• C/C++</li><li>• Bash</li><li>• Python</li><li>• Java</li><li>• Makefile/Cmake</li></ul>
<b>Embedded categories</b>	<ul style="list-style-type: none"><li>• Analog/Digital/Rf module design</li><li>• Firmware Design</li><li>• Device drivers</li><li>• Board bring up</li><li>• Software stack development</li><li>• Yocto build system environment</li><li>• Embedded Linux customization and development</li><li>• Automotive software</li><li>• Security in embedded systems&lt;</li></ul>
<b>Tools</b>	<ul style="list-style-type: none"><li>• Eclipse based IDE</li><li>• JIRA and other bug/issue tracking tools</li><li>• Skilled in different software versioning tools</li><li>• Code review</li><li>• Altium, hardware design environment</li><li>• Measurement equipment expertise</li></ul>





## Different Levels and Approaches

Our embedded experts are always ready for the next challenge. With years of experience in different industries and our skill set, we are at the forefront of embedded system innovations. Starting from specification, to the final turn-key embedded system design, we are following the latest technologies and using reliable tools and methodologies.

Our design principles are:

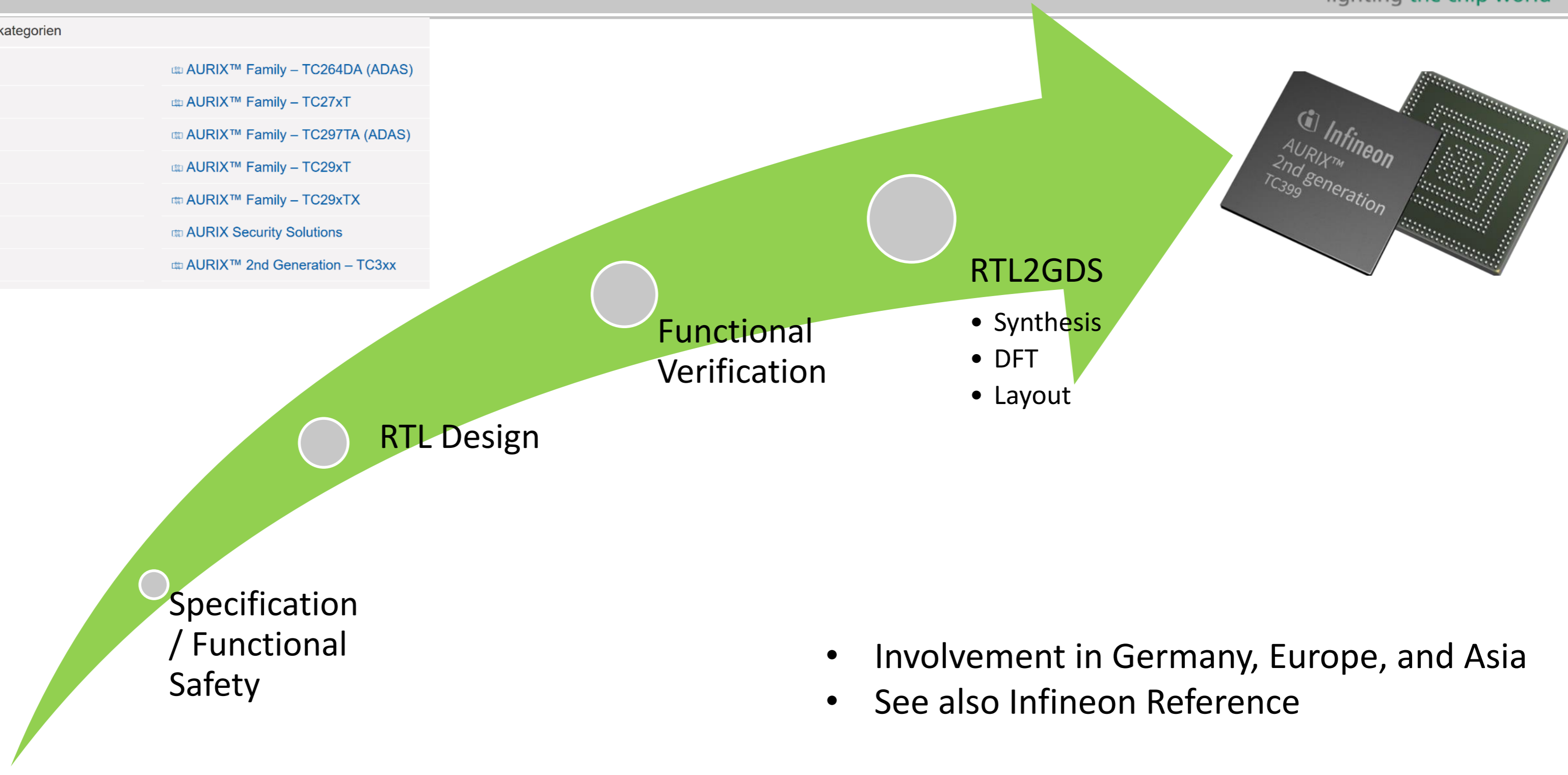
- test driven development
- Clean high-quality code
- Design patterns
- Strong team collaboration



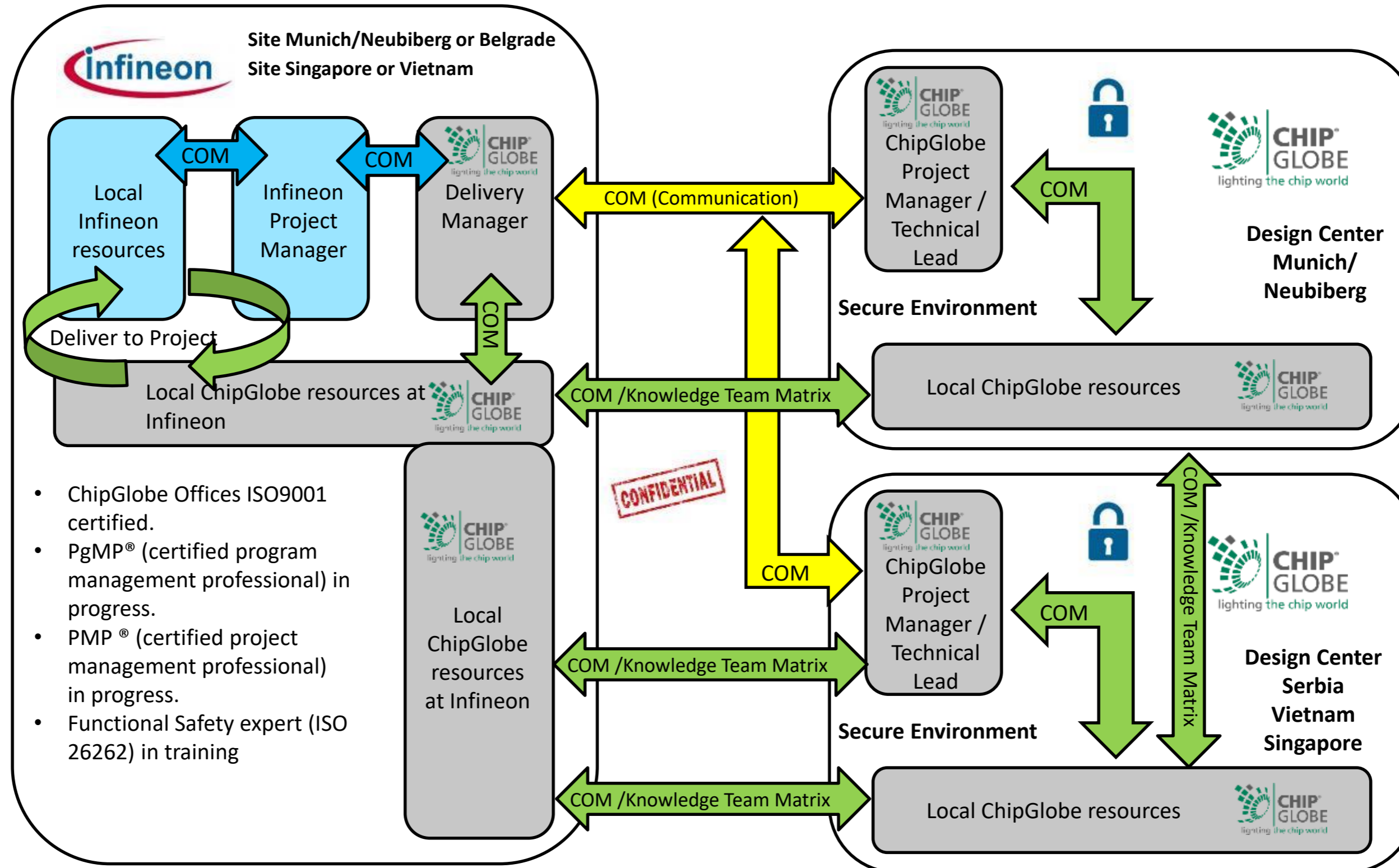
# ChipGlobe Automotive Aurix Family Involvement

AURIX™ – Safety joins Performance Unterkategorien

<ul style="list-style-type: none"> <li>AURIX™ Family – TC23xLA (ADAS)</li> <li>AURIX™ Family – TC23xLX</li> <li>AURIX™ Family – TC21xL</li> <li>AURIX™ Family – TC21xSC</li> <li>AURIX™ Family – TC22xL</li> <li>AURIX™ Family – TC23xL</li> <li>AURIX™ Family – TC26xD</li> </ul>	<ul style="list-style-type: none"> <li>AURIX™ Family – TC264DA (ADAS)</li> <li>AURIX™ Family – TC27xT</li> <li>AURIX™ Family – TC297TA (ADAS)</li> <li>AURIX™ Family – TC29xT</li> <li>AURIX™ Family – TC29xTX</li> <li>AURIX Security Solutions</li> <li>AURIX™ 2nd Generation – TC3xx</li> </ul>
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# Proven Carefree Setup with ChipGlobe



- ChipGlobe Offices ISO9001 certified.
- PgMP® (certified program management professional) in progress.
- PMP® (certified project management professional) in progress.
- Functional Safety expert (ISO 26262) in training



# ChipGlobe in the News - Forbes Asia – July / August 2018



As Europe's leading economic powerhouse and the world's fourth-largest economy, Germany has shown the world its winning formula: strong investment, low interest rates and high consumer spending. At the heart of that strength is Frankfurt, which is positioning itself as Europe's next financial capital to replace London in the post-Brexit era.

"We have close partnerships with financial sectors across Asia, including close and cordial working relationships with Tokyo and Singapore. And that is something which we are very happy about because we believe the future belongs to Asia," Frankfurt Main Finance Managing Director Hubertus Vath said.

Aside from Frankfurt, the federal state of Bavaria, home to some of the world's biggest global brands, continues to assert its dominance over the German economy.

"The GDP per capita of Munich is 72,000 euro, while Germany's is 40,000 euro. And if you look at the figures from the south of the country, this part of the Germany has become synonymous to Bavaria," said Bavarian Chamber of Commerce and Industry President Eberhard Sasse.

To maintain its leadership in Germany and the world, the public and private sectors in the region must work much closely together, according to Sasse.

In fact, Munich has already begun to diversify its economy beyond its traditional industrial sector and has ventured beyond Germany's national borders.

"Business and success should always be people driven and not just technology driven. Locally and globally, communication, transparency, respect and care is key to everything. Doing cross-border business and building global companies requires passion, partnerships and most of all, people," CM-Equity Founder and CEO Michael Kott said.

Over the past decades, German en-

gineering has become the benchmark across the globe. Many have attributed this competitive edge to the ability of German companies to adapt quickly to market requirements and their openness to customer feedback.

ChipGlobe, a German consulting company in the semiconductor industry, embodies this strategic and logical approach and combines it with a commitment to the success of its customers.

Founded by Volker Frisch in Munich in 2014, ChipGlobe hires highly experienced engineers who can design completely customizable solutions for its clients. This mission forms ChipGlobe's corporate culture and is the foundation of its success.

"You can only be successful if you have the right vision and value system," stressed Business Development Director Dieter Rudolf.

Detecting growth opportunities in Asia early on, ChipGlobe set up a subsidiary in Singapore in 2015. And after opening an outsource design center (ODC) in Belgrade in 2017, the company has begun construction of a new ODC in Ho Chi Minh City, Vietnam.

"We combine the strengths of German and Asian systems of quality, culture and values. If you look at the large companies in Germany, they try to reduce costs, sometimes through offshoring. If you look at places like Serbia,

you have a lower cost structure but still have quality talent. The same applies to Vietnam. The long-term trend is to focus on Asia and that's why we're opening a new ODC and investing there," Rudolf added.

Software giant SAP is another southern German company that recognizes that its success came only by prioritizing its customers.

"We aim to look at business challenges through the eyes of our customers first and how they are doing in servicing their own customers," explained CEO Bill McDermott.

With experience across 25 industries and operations in 193 countries, SAP closes the gap between the application of innovative technologies, such as machine learning and artificial intelligence, and the availability of predictive applications, process and insights that are in value chains to drive up productivity.

"SAP is the one company that can put it all together in a highly coherent, altruistic, purpose-driven way," McDermott said.

Looking ahead, Germany will continue to set the pace of European growth and develop closer ties with the Asia-Pacific. With its robust financial sector, political stability and well-developed infrastructure, the country will continue to be an ideal destination for Asian investment. ■







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Your letter	
Our sign	
Date	02.07.2018

To Whom it may concern,

"ChipGlobe has been a reliable and trusted supplier of Infineon Technologies AG for more than 15 years and has contributed to many successful ASIC implementations. They have been working for Infineon in several projects in different Infineon business units. This has resulted in reduced costs and increased efficiency. The partnership with their high level experts is based on sustainability – keeping the project specific knowledge within the ChipGlobe Design Center and Infineon R&D. Setup with Infineon's R&D teams was driven by easy interaction – same time zone, short travel time for personal meetings and closely aligned processes. ChipGlobe experts were committed to flexibility and the ability to react quickly on changes in demand. Infineon is collaborating with ChipGlobe internationally with their offshore design centers in Europe, as well as for onsite services in Singapore. ChipGlobe has been working on Infineon's automotive chip developments for more than 10 years, especially on the proven worldwide design support for the AURIX family. Their expertise in RTL2GDS and verification contributed to timely and sustainable ASIC roll-outs."

Please contact us at any point should you have questions about this recommendation.

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## Infineon reference for ChipGlobe



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# Infineon Supplier Award – November 2018



## ChipGlobe is Preferred Supplier at Infineon

- Top QoR (Quality of Results)
- Excellent Delivery in Time
- Proven Sustainability
- Excellent Teamwork
- Great Flexibility
- 15+ years proven partnership

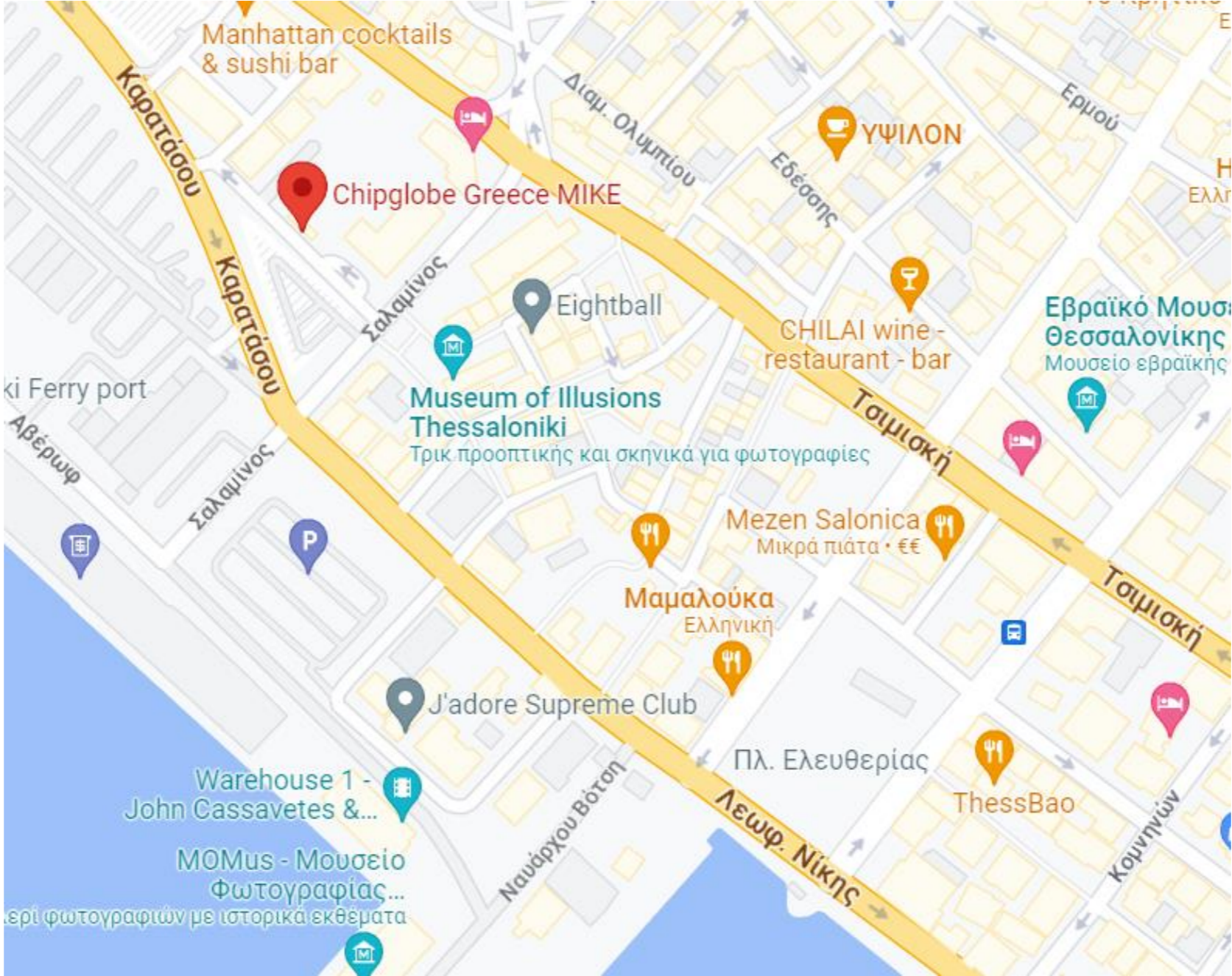


### From left to right:

- Volker Buttermann, Senior Director Purchasing at Infineon Technologies AG
- Volker Frisch, CEO at ChipGlobe GmbH
- Thomas Rühlicke, Senior Director SoC Design and Methodology at Infineon Technologies AG
- Roland Klemt, Managing Director at ChipGlobe GmbH



# ODC Thessaloniki – In the city center and close to the port





## Next steps

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Vietnam



What can we do  
to make you successful?

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